DETAILED ACTION

Preliminary Amendment

1.   Acknowledgement is made of the amendment filed by the applicant on June 27, 2006, in which claims 4-5, 9-10, and 14-15 are amended. Claims 1-15 are currently pending in U.S. Patent Application No. 10/596,846 and an office action on the merits follows.

Priority

2.   Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Claim Objections

3.   Claims 5, 10 and 15 are objected to because the claim language is unclear, although the examiner can understand what was meant.

4.   Regarding claims 5, 10 and 15, the phrase, "less a setting up time…" is unclear because it is not descriptive of relationship between the total duration of the row selection pulses and a setting time for a frame. For the purpose of examination, "less a setting up time..." will be interpreted as "less than a setting up time..." Appropriate correction is required.

Claim Rejections - 35 USC § 112

5.   The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6.   Claim 7 recites the limitation "the processor" in line 2. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

7.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the

basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8.   Claims 1-3, 6-8, and 11-13 are rejected under 35 U.S.C. 102(b) as being anticipated by

Matsuura et al (US 6,175,351, hereinafter Matsuura).

        Regarding claim 1, Matsuura discloses a display controller (control circuit 80, Fig. 12),

comprising: a processor (control circuit 80, Fig. 12) for providing row selection signals (Fig. 14)

for a display (display 100, Fig. 12) comprising M rows of pixels, wherein the row selection

signals comprise a respective row selection pulse (P1, P2, P3…Pm, Fig. 14) for each row, and

the row selection pulses have respective durations (t1, t2, t3. . . tm) that increase from the pulse

for row 1 to the pulse for row M, the increase in the pulse duration being one of the following:

(a) on a row-by-row basis (col. 22, lines 56-67; col. 23, lines 1-30); or (b) on a set of rows-by-set

of rows basis, where a set of rows comprises plural consecutive rows; or (c) on a mixture of a

row-by-row basis and a set of rows-by-set of rows basis, where a set of rows comprises plural

consecutive rows.

        Regarding claim 2, Matsuura discloses a display controller according to claim 1, wherein

the processor (80, Fig. 12) is further for receiving image data (R, G, B, Fig. 12) for the display,

and retiming the image data (40, Fig. 12; col. 21, lines 49-51; the time-axis modulation circuit 40

changes the timing of the image data when the image data is read from the memory 30) for

synchronization with the increase in the row selection pulse duration (col. 21, lines 46-56; Fig. 14).

Regarding claim 3, Matsuura discloses a display controller according to claim 2, further comprising a buffer (30, Fig. 12; the memory 30 stores the input image signal and outputs the retimed image data to the data transfer circuit 60), wherein the buffer (30) and the processor (80) are arranged for the processor (80) to retime the data by writing incoming data (20R, 20G, 20B) in to the buffer (30, col. 22, lines 1-6) at the rate the incoming data (20R, 20G, 20B) is received and reading the data out from the buffer (30) at a row rate corresponding to the increase in the row selection pulse duration (Fig. 14; col. 21, lines 46-56; col. 22, lines 46-56).

Regarding claim 6, Matsuura discloses a display device (Fig. 12), comprising an array of pixels arranged in M rows and N columns, a row driver circuit (data scanning circuit 70), and a display controller (control circuit 80), the display controller (80) being arranged to provide row selection pulses (P1, P2, P3…Pm) to the row driver circuit (70), the row selection pulses (P1, P2, P3…Pm) having respective durations (t1, t2, t3 . . . tm) that increase from the pulse for row 1 to the pulse for row M, the increase in the pulse duration being one of the following: (a) on a row-by-row basis(col. 22, lines 56-67; col. 23, lines 1-30); or (b) on a set of rows-by-set of rows basis, where a set of rows comprises plural consecutive rows; or (c) on a mixture of a row-by-row basis and a set of rows-by-set of rows basis, where a set of rows comprises plural consecutive rows.

Regarding claim 7, Matsuura discloses a display device according to claim 6, wherein the processor (80) is further for receiving image data (R, G, B, Fig. 12) for the display, and retiming the image data (40, Fig. 12; col. 21, lines 49-51, the time-axis modulation circuit 40 changes the

timing of the image data when the image data is read from the memory 30) for synchronization

with the increase in the row selection pulse duration (write time modulation circuit 82, Fig. 12;

col. 21, lines 46-57; col.22, lines 47-56).

Regarding claim 8, Matsuura discloses a display device according to claim 7, further

comprising a buffer (memory 30, Fig. 12; the memory 30 stores the input image signal and

outputs the retimed image data to the data transfer circuit 60), wherein the buffer (30) and the

processor (80) are arranged for the processor (80) to retime the data by writing incoming data (R,

G, and B signals, Fig. 12) into the buffer (30) at the rate the incoming data is received (col. 22,

lines 1-29) and reading the data out from the buffer (col. 21, lines 49-56) at a row rate

corresponding to the increase in the row selection pulse duration (Fig. 14).

Regarding claim 11, Matsuura discloses a method of driving a display device (Fig. 12),

the display device comprising an array of pixels arranged in M rows and N columns, the method

comprising: providing row selection pulses (P1, P2, P3…Pm, Fig. 14) to each row in turn, the

row selection pulses (P1, P2, P3…Pm) having respective durations (t1, t2, t3 . . . tm, Fig. 14) that

increase from the pulse for row 1 to the pulse for row M, the increase in the pulse duration being

one of the following: (a) on a row-by-row basis (col. 22, lines 56-67; col. 23, lines 1-30); or (b)

on a set of rows-by-set of rows basis, where a set of rows comprises plural consecutive rows; or

(c) on a mixture of a row-by-row basis and a set of rows-by-set of rows basis, where a set of

rows comprises plural consecutive rows.

Regarding claim 12, Matsuura discloses a method of driving a display device according

to claim 11, further comprising retiming image data (time-axis modulation circuit 40, Fig. 12;

col. 21, lines 49-51, the time-axis modulation circuit 40 changes the timing of the image data

when the image data is read from the memory 30) for synchronization with the increase in the

row selection pulse duration (col. 21, lines 46-56; Fig. 14)

Regarding claim 13, Matsuura discloses a method of driving a display device according

to claim 12, wherein the step of retiming image data comprises writing incoming data (R, G, and

B image signals, Fig. 12) in to a buffer (memory 30 stores the input image data and outputs the

retimed image data into the data transfer circuit 60, col. 21, lines 46-56) at the rate the incoming

data is received and reading the data out from the buffer (30) at a row rate corresponding to the

increase in the row selection pulse (Fig. 14).

Claim Rejections - 35 USC § 103

9.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in
> section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are
> such that the subject matter as a whole would have been obvious at the time the invention was made to a person
> having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the
> manner in which the invention was made.

10.   Claims 4, 9 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Matsuura et al (US 6175351, hereinafter Matsuura) in view of Lee et al (US 2003/0038766,

hereinafter Lee).

Regarding claim 4, Matsuura discloses a display controller according to claim 1.

Matsuura fails to disclose wherein the number of rows in a given set is less than the number of

rows in one or more preceding sets. However, Lee discloses a display controller (time controller

400, Fig. 1) similar to Matsuura. Lee further discloses the display controller providing row

selection signals (e.g. scanning signals g, Fig. 4) to a first set of consecutive rows (g4i+2, g4i+3,

g4(i+1) and a second set of consecutive rows (g4(i+1)+1) with different durations, respectively.

The number of rows in the second set is one row which is less than the three rows in the

preceding set such as the first set. Therefore, it would have been obvious to one of ordinary skill

in the art at the time the invention was made to modify Matsuura with the features of different set

of rows having different scanning period as taught by Lee so as to provide a multiple lines

scanning within a time frame period.

Regarding claim 9, this claim is rejected under the same rationale as claim 4.

Regarding claim 14, this claim is rejected under the same rationale as claim 4.

11.   Claims 5, 10 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Matsuura et al (US 6175351, hereinafter Matsuura) in view of Ozawa et al (US 6,501,454,

hereinafter Ozawa).

Regarding claim 5, Matsuura discloses a display controller according to claim 1, wherein

the total duration of the row selection pulses for all the rows is substantially equal to a frame

time (Fig. 16, col. 14, lines 57-60; col. 23, lines 49-58). It is noted that Matsuura fails to

disclose that the total duration of the row selection pulses for all the rows is less than a setting up

time for a frame of the display. However, Ozawa discloses a scanning driver (Fig. 4) wherein

the total duration of row selection pulses (e.g. total duration of T3, Fig. 4) for all rows is less

than a setting time (e.g. total duration of T1, Fig. 4) for a frame of a display (see col. 8, lines 37-

52). Therefore, it would have been obvious to one of ordinary skill in the art at the time the

invention was made to combine the display controller of Matsuura with the feature of the setting

period (or resetting period) as taught by Ozawa such that the power consumption does not

increase (see abstract of Ozawa, lines 9-25).

Regarding claim 10, this claim is rejected under the same rationale as claim 5.

Regarding claim 15, this claim is rejected under the same rationale as claim 5.

Conclusion

12.   The prior art made of record and not relied upon is considered pertinent to applicant's

disclosure.

US 7,164,405, US 6,407,727, US 5,568,163 and US 2004/0021625 are cited to teach a

display controller for providing row selection signals.

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to HONG ZHOU whose telephone number is (571)270-5372. The

examiner can normally be reached on Monday through Friday 8:30 A.M. - 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Amare Mengistu can be reached on (571)272-7674. The fax phone number for the

organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent

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/H. Z./
Examiner, Art Unit 2629

/Amare Mengistu/

Supervisory Patent Examiner, Art Unit 2629